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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,890	02/09/2004	Biswajit Sur	884.319US2	1421

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,890	SUR ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *1-3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to the Restriction Requirement dated September 28, 2004, Applicant has elected, without traverse, Group II (claims **4-29)** is acknowledged. Accordingly, claims **1-3** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **1-3**.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 02/09/2004. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **4-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Daves et al. (USP: 6,091,603 hereinafter referred to as "Daves") in view of Edwards et al. (USP: 6,294,408 hereinafter referred to as "Edwards").

Regarding claim **4**, Daves discloses in Fig. 2 a method comprises:

forming at least one thermally conductive, compliant material (200) on a surface of a die/chip (600);

mounting the die/chip on a substrate (500);

applying solder material (103) to the at least [one metal layer] one thermally conductive, compliant material;

positioning a surface of a lid adjacent the solder material; and

melting the solder material to physically couple the lid to the die (column 4, line 16-column 6, line 18).

Daves fails to teach forming at least one metal layer on a surface of a die.

However, Edwards teaches in Fig. 2 a metal thermal interface material (19) is used between chip device (16) and lid (20) as set forth in column 7, lines 6-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a metal thermal interface material between chip device and lid to enhance the thermal conductivity, as taught by Edwards to incorporate into the method of Daves to modify and to replace the step of forming at least one thermally conductive, compliant material on a surface of a die/chip with the step of forming at least one metal layer on a surface of a die to arrive the claimed limitation in order to enhance heat dissipation between the die and the lid.

Regarding claims **5 and 11**, Daves and Edwards disclose the claimed limitations except for the method wherein in applying the solder material, the solder material has a relatively high thermal conductivity and a relatively low melting point. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the solder material having a relatively high thermal conductivity and a relatively low melting point since it was known in the art that the solder material having a relatively high thermal conductivity and a relatively low melting point is used for cooling enhancement of the die/chip.

Regarding claims **6 and 12**, Daves discloses the method wherein, in mounting the die on the substrate, the substrate comprises organic material having a relatively high thermal coefficient of expansion relative to that of the die (col. 6, lines 14-17).

Regarding claims **7 and 15**, Daves and Edwards disclose the claimed limitations except for the method further comprising forming at least one metal or organic layer on the surface of the lid prior to positioning the surface of the lid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to further form at least one metal or organic layer on the surface of the lid prior to positioning the surface of the lid in order to additionally enhance heat dissipation between the die and the lid.

Regarding claim **8**, Daves discloses in Fig. 2 a method comprises:

forming an adhesion layer (200) on a surface of a die/chip (600);

forming a solder-wettable layer (104) on the adhesion layer;

mounting the die on a substrate;

applying solder material (103) to the solder-wettable layer;

positioning a surface of a lid (101) adjacent the solder material; and

melting the solder matedal to physically couple the lid to the die (column 4, line 16-column 6, line 18).

Daves fails to teach forming an adhesion layer of metal on a surface of a die.

However, Edwards teaches in Fig. 2 a metal thermal interface material (19) is used between chip device (16) and lid (20) as set forth in column 7, lines 6-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a metal thermal interface material between chip device and lid to enhance the thermal conductivity, as taught by Edwards to incorporate into the method of Daves to modify and to replace the step of forming at least one thermally conductive, compliant material on a surface of a die/chip with the step of forming an adhesion layer of metal on a surface of a die to arrive the claimed limitation in order to enhance the thermal conductivity of the adhesive layer.

Regarding claims **9, 10, 14, 16, 18, 20, 21, 24, 26, 27 and 29**, Daves and Edwards disclose the claimed limitations except for the method wherein the adhesion layer comprises material, including one or more alloys, from the group consisting of titantium, chromium, zirconium, nickel, vanadium, and gold; wherein the solder-wettable layer comprises one of nickel and gold; wherein the solder material comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead; wherein the at least one metal or organic layer, the at least one metal or organic layer comprises one of nickel and gold; wherein the diffusion layer comprises material, including one or more alloys, from the group consisting of titanium, chromium, zirconium, nickel, vanadium, and gold. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the adhesion layer comprising material, including one or more alloys, from the group consisting of

titantium, chromium, zirconium, nickel, vanadium, and gold; the solder-wettable layer comprising one of nickel and gold; the solder material comprising material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead; the at least one metal or organic layer, the at least one metal or organic layer comprising one of nickel and gold; the diffusion layer comprising material, including one or more alloys, from the group consisting of titanium, chromium, zirconium, nickel, vanadium, and gold, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim **13**, Daves discloses the method wherein, in positioning the surface of the lid, the lid comprises material from the group consisting of copper and aluminum-silicon-carbide (col. 4, lines 20-27).

Regarding claims **17, 23 and 28**, Daves and Edwards disclose the claimed limitations except for the method further comprises forming a diffusion layer between the adhesion layer and the solder-wettable layer. It would have been an obvious matter of design choice to form a diffusion layer between the adhesion layer and the solder-wettable layer, since applicant has disclosed in the specification, page 7, lines 29-30 that the diffusion layer is not necessarily required, depending upon the composition of the adhesion layer and it appears that the invention would perform equally well without the diffusion layer.

Regarding claim **19**, Daves discloses in Fig. 2 a method comprises:

forming an adhesion layer (200) on a back surface of a die/chip (600);

forming a solder-wettable layer (104) on the adhesion layer;

mounting another surface of the die on a substrate (500); and

applying solder material (103) to the solder-wettable layer (column 4, line 16-column 6, line 18).

Daves fails to teach forming an adhesion layer of metal on a back surface of a die.

However, Edwards teaches in Fig. 2 a metal thermal interface material (19) is used between chip device (16) and lid (20) as set forth in column 7, lines 6-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a metal thermal interface material between chip device and lid to enhance the thermal conductivity, as taught by Edwards to incorporate into the method of Daves to modify and to replace the step of forming at least one thermally conductive, compliant material on a surface of a die/chip with the step of forming an adhesion layer of metal on a back surface of a die to arrive the claimed limitation in order to enhance the thermal conductivity of the adhesive layer.

Regarding claim **25**, Daves discloses in Fig. 2 a method comprises:

forming an adhesion layer (200) on a surface of a die/chip (600); and

forming a solder-wettable layer (104) on the adhesion layer (column 4, line 16-column 6, line 18).

Daves fails to teach forming an adhesion layer of metal on a surface of a die.

However, Edwards teaches in Fig. 2 a metal thermal interface material (19) is used between chip device (16) and lid (20) as set forth in column 7, lines 6-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a metal thermal interface material between chip device and lid to enhance the

thermal conductivity, as taught by Edwards to incorporate into the method of Daves to modify and to replace the step of forming at least one thermally conductive, compliant material on a surface of a die/chip with the step of forming an adhesion layer of metal on a surface of a die to arrive the claimed limitation in order to enhance the thermal conductivity of the adhesive layer.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

10/15/04

Andy Huynh

Patent Examiner